**[0043]** The present invention includes a method and apparatus for measuring a parasitic inductance associated with a portion of an integrated circuit fabricated on a semiconductor substrate. A test chip for measuring the parasitic inductance is fabricated together with the integrated circuit on the semiconductor substrate. The test chip includes an LC oscillator circuit having at least one substructure that resembles the portion of the integrated circuit and at least one varactor having a capacitance adjustable by a control voltage. When the LC oscillator circuit is connected to the control voltage source and the control voltage is at a certain level, an oscillation is generated in the LC oscillator and the frequency of oscillation can be used to determine the parasitic inductance associated with the portion of the integrated circuit.